Amendments to the Specification

Please enter the following amendments (numbered 1-9) to the specification and Abstract.

1. Please replace the paragraph beginning at page 1, line 13, with the following rewritten paragraph:

In a wideband Code Division Multiple Access (CDMA) system, multiple paths of a transmitted signal can be tracked using a rake receiver implemented at a base station due to the nature of spread spectrum sequences in a wireless channel. The rake receiver functions as several receivers operating with associated propagation delays based on the respective delays experienced by arriving multipath signals. The rake receiver has a tracking loop for each rake finger of a user that tracks the movement of the fingers typically through the use of a delay locked loop (DLL). The DLL, which computes the error in, and subsequently shifts, the sample time, needs to be performed on a per finger, or multipath, basis.

2. Please replace the paragraph beginning at page 2, line 4, with the following rewritten paragraph:

In new high end devices, more processing is being moved to digital signal processors. In addition, the potential for performance improvements via more sophisticated software algorithms creates motivation to place more functions like DLL processing in software. However, this shift in processing puts a strain on Digital Signal Processor (DSP) bandwidth, as such bandwidth is typically small enough to create processing bottlenecks at the DSP I/O interface and therefore slow down DSP processing times.

3. Please replace the paragraph beginning at page 3, line 11, with the following rewritten paragraph:

FIG. 2 is a block diagram of a preferred embodiment of a post-correlation processing system according to the present invention; ~~and~~

4. Please replace the paragraph beginning at page 3, line 14, with the following rewritten paragraph:

FIG. 3 is a block diagram of a rake receiver using the post-correlation processing system shown in FIG. 2; and

5. Please add the following paragraph at page 3, line 17:

FIG. 4 is a flow chart illustrating a method of processing samples for delay locked loop processing.

6. Please replace the paragraph beginning at page 4, line 14, with the following rewritten paragraph:

Referring to FIG. 2, the post-correlation processing system 12 performs an essential function for delay locked loops and processing therein and includes an Input/Output (I/O) interface 14 for receiving input signal samples, preferably, CDMA chip samples such as those generated at a known analog processing circuit (FIG. 3) that samples received signals, preferably, CDMA received signals at, for example, two times the chip rate. The I/O interface 14 then distributes identical sets of these samples or input samples or chip samples to an interpolator 16, a first multiplexer 18, and a second multiplexer 20. Specifically, the I/O interface 14 distributes the chip samples directly to the interpolator through an interpolator input 16a and also directly to the first and second multiplexers 18, 20 through first and second multiplexer inputs 18a, 20a, respectively. The interpolator 16 is known and introduces a time offset to the input chip samples and interpolates between the input chip samples to increase chip resolution from, for example, 1/2 chip resolution if the chip samples are sampled at two times the chip rate to, for example, 1/8 chip resolution. The interpolator 16 thereby recovers time shifted samples or chip samples that

are shifted in time relative to the chip samples from the I/O interface 14. Note that if or when the time reference (not shown) used to generate the samples or chip samples from I/O interface 14 is in phase or synchronized or nearly so with a desired CDMA spreading sequence these chip samples from I/O interface 14 will be "ontime" samples or "ontime" chip samples and the time shifted samples or time shifted chip samples recovered by interpolator 16 will then be non-ontime samples or non-ontime chip samples according to the conventions used within this disclosure. It follows that non-ontime is a general reference to either late or early samples or chip samples that are not in phase with any CDMA spreading sequences for any users/subscribers. In any event the recovered time shifted (whether non-ontime or ontime) chip samples are then distributed to both the first and the second multiplexers 18, 20 through multiplexer inputs 18b, 20b.

7. Please replace the paragraph beginning at page 9, line 8, with the following rewritten paragraph:

FIG. 3 shows, in block diagram form, a preferred embodiment of an exemplary implementation of the post-correlation processing system in a rake receiver 30, such as may be utilized in a CDMA receiver for a cellular base station. However, it should be appreciated that this specific implementation is exemplary only, as the post-correlation processing system of the present invention may be implemented in any type of environment in which correlation functions must be processed, such as, for example, fast hopped spread spectrum communications systems as well as mobile handsets or radios within a CDMA system. Specifically, an analog processing circuit 32 removes the carrier frequency from a signal, such as a CDMA signal received by an antenna 34 and samples the received CDMA signal at a predetermined sampling rate, such as twice the chip rate, to produce corresponding CDMA chip samples. The CDMA chip samples are input into a correlator Application-Specific Integrated Circuit (ASIC) 36 in which, according to this specific configuration, all of the components of the post-correlation processing system 12 of the present invention are implemented, including the DSP for implementing, either via hardware or software, the postcorrelation processor 28. Alternatively, if the post-correlation

processing system 12 of the present invention is utilized within, for example, a mobile handset environment, the components implemented within the ASIC 36 could alternatively be software implemented. The correlator ASIC 36 outputs generated ontime and non-ontime symbol samples to a DSP buffer 40 in which the early, late and ontime symbol samples E, L, O are stored before being input into a processor 42, such as a Motorola 8102 base station processor, for additional processing including DLL, symbol rate, and chip rate processing as is known in the art.

8. Please add the following paragraph beginning at page 10, line 1, after the description of FIG. 3:

FIG. 4 depicts a flow chart illustrating a method 50 of processing samples for delay locked loop processing. The method 50 starts at 52 and then shows interpolating 54 between received samples to generate time shifted samples, e.g., received CDMA chip samples to generate time shifted CDMA chip samples. The method further includes extracting 56 ontime control symbol samples from one of the received samples (e.g., CDMA chip samples) and the time shifted samples (e.g., time shifted CDMA chip samples) and extracting 58 first non-ontime control symbol samples from one of the received samples and the time shifted samples. Furthermore, the method includes subsequently extracting 60 second non-ontime symbol samples based on the first non-ontime control symbol samples and the ontime control symbol samples. In one embodiment the subsequently extracting 60 can include subsequently interpolating, at a symbol rate, the first non-ontime control symbol samples and the control symbol samples to provide the second non-ontime symbol samples. As suggested above, the received samples can be CDMA chip samples and the time shifted samples can be time shifted chip samples.

9. Please replace the Abstract with the enclosed Replacement Abstract.